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PTO/SB/21 (07-06)

Approved for use through 09/30/2006. OMB 0651-0031

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**TRANSMITTAL
FORM**

(to be used for all correspondence after initial filing)

TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	Patent#: 7,113,031	
	Filing Date	Issued: September 26, 2006	
	First Named Inventor	Vincent Rabary	
	Art Unit	2819	
	Examiner Name	L. T. Mai	
Total Number of Pages in This Submission	6	Attorney Docket Number	S1022.81105US00

ENCLOSURES (Check all that apply)

<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input checked="" type="checkbox"/> Request for Certificate of Correction <input checked="" type="checkbox"/> Certificate of Correction <input checked="" type="checkbox"/> Page 2 of 04/11/06 Amendment <input checked="" type="checkbox"/> Column 6 of U.S. Patent No. 7,113,031 <input type="checkbox"/> Reply to Missing Parts/Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please Identify below): Return Receipt Postcard
Remarks		
Certificate OCT 11 2006 of Correction		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	WOLF, GREENFIELD & SACKS, P.C.		
Signature	<i>William R. McClellan</i>		
Printed name	William R. McClellan		
Date	October 4, 2006	Reg. No.	29,409

Certificate of Mailing Under 37 CFR 1.8(a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: October 4, 2006

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<input checked="" type="checkbox"/> Column 6 of U.S. Patent No. 7,113,031	<input type="checkbox"/> Landscape Table on CD	
<input type="checkbox"/> Reply to Missing Parts/Incomplete Application	Remarks	
<input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	WOLF, GREENFIELD & SACKS, P.C.		
Signature	<i>William R. McClellan</i>		
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Signature: *Gail Driscoll* (Gail Driscoll)

OCT 12 2006



Docket No.: S1022.81105US00
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Vincent Rabary et al.
Serial No.: 10/816,126 Patent No. 7,113,031
Filed: April 1, 2004 Issued: September 26, 2006
For: AUDIO AMPLIFIER CIRCUIT WITH SUPPRESSION OF
UNWANTED NOISE WHEN POWERED ON FROM STANDBY

Examiner: L. T. Mai
Art Unit: 2819 Confirmation No. 9639

Certificate of Mailing Under 37 CFR 1.8(a)

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Dated: October 4, 2006

Gail Driscoll
Gail Driscoll

**REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322**

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted typographical errors which should be corrected.

In the claims:

In claim 1, column 6, line 13 of U.S. Patent No. 7,113,031 the text reads:

amplifier having a single output, a first input receiving an

However, in the amendment mailed April 11, 2006 the corresponding text read:

amplifier having a single output, **having** a first input receiving an (Emphasis added)

OCT 12 2006

In claim 4, column 6, line 29 of U.S. Patent No. 7,113,031 the text reads:

amplifier, wherein a second amplifier receives at a first input (Emphasis added)

However, in the amendment mailed April 11, 2006 the corresponding text read:

amplifier, wherein **the** second amplifier receives at a first input (Emphasis added)

The errors listed above were not in the claims as listed in the amendment filed by Patentee on April 11, 2006, nor was there an Examiner's amendment making such changes to the claims.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

In support of the above, Patentees enclosed highlighted copy of the April 11, 2006 amendment and column 6 of U.S. Patent No. 7,113,031.

Patentees respectfully submit that, since the errors for which a Certificate of Correction is sought were the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: October 4, 2006

Respectfully submitted,

By: William R. McClellan

William R. McClellan

Registration No.: 29,409

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OCT 12 2006

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currents, for example, in load Q, and/or in the different off switches. As illustrated in dotted lines in the timing diagrams of FIGS. 4B to 4D, nodes BP, S, and M, respectively, are then maintained at reference voltage V_{ref} . Output voltage V_{out} across load Q remains always stable, at zero, as illustrated in FIG. 4E, and the occurrence of residual noise is suppressed.

The occurrence of unwanted noise at the exit from a standby state of an amplifier circuit has been described previously in relation with a structure comprising a single operational amplifier 10. However, this problem also appears in a so-called bridge tiled load (BTL) structure with two operational amplifiers in cascade to which the present invention also applies.

FIG. 5 illustrates another embodiment of the present invention, applied to such a bridge assembly. The amplifier circuit comprises amplifier 10 and all its peripheral elements described in relation with FIG. 1, except for output decoupling capacitor 14, which is eliminated. Output O1 of amplifier 10 is then directly connected to a terminal of load Q having its other terminal connected to output O2 of a second operational amplifier 30. Second amplifier 30 is assembled as an inverter. The inverting input (-) of amplifier 30 is connected to output O1 of amplifier 10 by a resistor 31 and to its output O2 by a resistor 32. The non-inverting input (+) of amplifier 30 is connected to node BP that forms the non-inverting input of the amplifier circuit.

Node BP is connected, as described previously in relation with FIG. 1, to the midpoint of a resistive dividing bridge. However, as illustrated in FIG. 5, the dividing bridge further comprises a controllable switch 33 between resistor 16 and ground GND. Switch 33 is a switch of the same control logic as switch 17. In the shown example, switch 33 is controlled by inverse NSB of signal SB, switch 17 being a P-channel MOS transistor and switch 33 being an N-channel MOS transistor.

According to the embodiment of FIG. 5, the bridge-assembled amplifier circuit further comprises switch 20 interconnecting terminals M and BP.

As compared to the architecture of FIG. 3, switch 21 is eliminated. Indeed, switch 21 is not necessary in the absence of output decoupling capacitor 14. The decoupling capacitor is no longer necessary in the bridge assembly of FIG. 5, given that the D.C. components of amplifiers 10 and 30 compensate for each other.

The presence of switch 20 according to a feature of the present invention enables, as previously discussed in relation with FIG. 3 for an assembly with a single amplifier 10, stabilizing the charges of coupling and decoupling capacitors 12 and 18 by balancing their discharge. Further, the introduction of switch 33 enables, as discussed in relation with the alternative of FIG. 3, avoiding discharge of the capacitors through resistor 16. Voltages V_M and V_{BP} are thus equal to reference level V_{ref} (neglecting leakage) at the end of a standby.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. In particular, those skilled in the art will be able to choose elements capable of implementing the desired operation. For example, operational amplifiers 10 and 30 may be replaced with any element performing the same function. Similarly, those skilled in the art will be able to appropriately choose and control switches 17, 20, 21, and 33. The switches have been previously described as being switches controllable to be turned on and to be turned off. They may however be

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normally-on or off switches controllable to be turned off or to be turned on by signal SB.

Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

1. A power amplifier circuit comprising at least one first amplifier having a single output, a first input receiving an input voltage through at least one first coupling capacitor and connected to the single output of the first amplifier, and having a second input, separate from the first input, receiving a reference voltage supplied by a time constant circuit comprising a decoupling capacitor, at least one first controllable switch connecting the first and second inputs wherein the first controllable switch connects the first and second inputs together when in an on state.

2. The circuit of claim 1, wherein the first controllable switch connects directly the first and second inputs.

3. The circuit of claim 1, wherein the output of the first amplifier is connected to a load by a second coupling capacitor, at least one second controllable switch connecting the output and the first input.

4. The circuit of claim 1, further comprising a second amplifier, wherein a second amplifier receives at a first input the outputs of the first and second amplifiers, the second inputs of the first and second amplifiers being interconnected, the outputs of the first and second amplifiers being connected to respective terminals of a load.

5. The circuit of claim 1, wherein the second input is connected to the midpoint of a series connection between high and low supply terminals of first and second resistors.

6. The circuit of claim 5, wherein at least one second controllable switch, controlled at the same time as the first controllable switch, is interposed between the second resistor and the low supply terminal.

7. The circuit of claim 6, wherein a third controllable switch, controlled by a same signal as the first controllable switch, and of inverse control logic, is interposed between the high supply terminal and the first resistor.

8. A power amplifier circuit comprising:

a first amplifier having a first input, a second input and a single output;

a first coupling capacitor, connected to the first input, for receiving an input voltage;

a reference voltage circuit for supplying a DC reference voltage to the second input; and

a controllable switch connected between the first and second inputs, wherein the controllable switch connects the first and second inputs together when in an on state.

9. A power amplifier circuit as defined in claim 8, further comprising a second coupling capacitor for coupling the output of the first amplifier to a load and a second controllable switch connected between the output and the first input.

10. A power amplifier circuit as defined in claim 9, further comprising a feedback element connected between the output and the first input.

11. A power amplifier circuit as defined in claim 8, wherein the reference voltage circuit comprises first and second resistors forming a resistive divider, a junction point of the resistive divider connected to the second input, the

AMENDMENTS TO THE CLAIMS

Please replace all prior versions of claims in the application with the following list of claims:

1. (Currently amended) A power amplifier circuit comprising at least one first amplifier having a single output, having a first input receiving an input voltage through at least one first coupling capacitor and connected to the single ~~an~~ output of the first amplifier, and having a second input, separate from the first input, receiving a reference voltage supplied by a time constant circuit comprising a decoupling capacitor, at least one first controllable switch connecting the first and second inputs, wherein the first controllable switch connects the first and second inputs together when in an on state.
2. (Original) The circuit of claim 1, wherein the first controllable switch connects directly the first and second inputs
3. (Original) The circuit of claim 1, wherein the output of the first amplifier is connected to a load by a second coupling capacitor, at least one second controllable switch connecting the output and the first input.
4. (Previously presented) The circuit of claim 1, further comprising a second amplifier, wherein the second amplifier receives at a first input the outputs of the first and second amplifiers, the second inputs of the first and second amplifiers being interconnected, the outputs of the first and second amplifiers being connected to respective terminals of a load.
5. (Original) The circuit of claim 1, wherein the second input is connected to the midpoint of a series connection between high and low supply terminals of first and second resistors.
6. (Original) The circuit of claim 5, wherein at least one second controllable switch, controlled at the same time as the first controllable switch, is interposed between the second resistor

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

Page 1 of 1

PATENT NO. : 7,113,031
APPLICATION NO. : 10/816,126
ISSUE DATE : September 26, 2006
INVENTOR(S) : Vincent Rabary and Frédéric Goutti

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 1, column 6, line 13 of U.S. Patent No. 7,113,031 should read:
amplifier having a single output, having a first input receiving an

Claim 4, column 6, line 29 of U.S. Patent No. 7,113,031 should read:
amplifier, wherein the second amplifier receives at a first input

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OCT 12 2006